PATENT ABSTRACTS OF JAPAN

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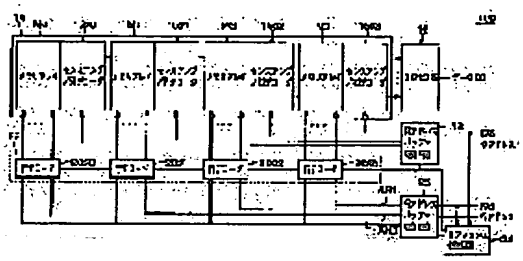
(54) SEMICONDUCTOR MEMORY

(57)Abstract:
PROBLEM TO BE SOLVED: To enable specifying efficiently a row address corresponding to refresh operation by decoding an output of a shift register outputting an internal address outputted by an address control circuit as it is and selecting a corresponding word line.
SOLUTION: A refresh control circuit 24 generates a signal responding to control signals RAS, CAS and controlling refresh. A row address buffer control circuit 25 outputs internal row address signals AR0, AR1 of high-order and low-order by a control signal RAS and an external address. In a normal mode, the address signal AR0 specifies a corresponding memory array and the signal AR1 specifies a word line. Row decoders 20#0-20#3 of a row decoder section 22 are corresponding to memory arrays M0-M3, the row decoder section 22 comprises a shift register, a semiconductor storage device 100 substitutes for a binary counter, a shift register being an address specifying circuit selects a memory array and a word line being object of a refresh operation mode.



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